AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-14 (Canceled without prejudice or disclaimer).

15. (Currently Amended) A semiconductor device comprising:

a functional circuit block for performing a processing when an instruction or data is inputted,

a power status control circuit for controlling a power status of said functional circuit block, and

a prediction circuit coupled to receive the instruction or data for controlling said power status control circuit, independently of other computation devices, based on said instruction or data and on an interval between successive instructions or data which ~~is~~ are inputted to both the functional circuit block and the prediction circuit.

16. (Previously Presented) A semiconductor device according to claim 15,

wherein said prediction circuit has a function to control said functional circuit block to process said instruction or data inputted into said functional circuit block.

17. (Previously Presented) A semiconductor device according to claim 15,

wherein said power status control circuit comprises at least a power shutdown circuit, or an operating voltage setting circuit, and/or an operating frequency setting circuit,

wherein clock pulses are inputted into said functional circuit block and said power status control circuit;

wherein, when there is an input to said functional circuit block, said power shutdown circuit supplies a power to said functional circuit block, said operating voltage setting circuit sets an operating voltage supplied to said functional circuit block to a first voltage, and said operating frequency setting circuit sets an operating frequency of said functional circuit block to a first frequency, and

wherein, when there is no input to said functional circuit block for a period in which said power status control circuit counts said clock pulses n times, said power shutdown circuit shuts down a power supplied to said functional circuit block, said operating voltage setting circuit sets said operating voltage supplied to said functional circuit block to a second voltage lower than said first voltage, and said operating frequency setting circuit sets said operating frequency of said functional circuit block to a second frequency lower than said first frequency.

18. (Currently Amended) A semiconductor device according to claim 15,

wherein said power status control circuit comprises a power shutdown circuit for shutting down power which is supplied to said functional circuit block, said power shutdown circuit being coupled to said functional circuit block and a power supply,

wherein clock pulses are inputted into said functional circuit block and said power status control circuit,

wherein said prediction circuit comprises a counter for counting the number of clock pulses inputted to said functional circuit block and to said counter, a control circuit for controlling said power shutdown circuit, and an input detection circuit receiving the instruction or data inputted to said functional circuit block for detecting said instruction or data inputted to said functional circuit block,

wherein said counter outputs a first signal to said control circuit when a number of said clock pulses counted is n, and

wherein, when there is no instruction or data inputted to said functional circuit block, said input detection circuit outputs a reset signal to said counter to reset a counting of said clock pulses and outputs a second signal to said control circuit, and said control circuit outputs an output signal of a first state to shut down said power supplied to said functional circuit block when both said first and second signals are inputted to said control circuit.

19. (Previously Presented) A semiconductor device according to claim 18,

wherein said functional circuit block comprises a register for temporarily storing said instruction or data and a functional block for computation, and

wherein said prediction circuit further comprises a comparator for controlling said register by comparing the output of said control circuit with the number of clock pulses inputted to said comparator and a predetermined number, said comparator

starting a counting of said clock pulses when said control circuit outputs said output signal of a second state.

20. (Currently Amended) A semiconductor device according to claim 15,

wherein clock pulses are inputted into said functional circuit block, said power status control circuit block comprises an operation voltage setting circuit for setting an operating voltage of said functional circuit block, said operation voltage setting circuit being coupled to said functional circuit block and a power supply,

wherein said prediction circuit comprises a first switch provided between a first control signal line and said operating voltage setting circuit, said first control signal line supplying a first signal voltage to said operating voltage setting circuit, a second switch provided between a second control signal line and said operating voltage setting circuit, said second control signal line supplying a second voltage lower than said first signal voltage to said operating voltage setting circuit, and a switch control circuit inputted with said instruction or data and said clock pulses and controlling said first and second switches, and

wherein, when said data or instruction is inputted to said functional circuit block, said switch control circuit controls the first switch to supply said first signal voltage to said operating voltage setting circuit and, when said switch control circuit counts said clock n times after said data or instruction is inputted to said functional circuit block, said switch control circuit controls said second switch to supply said second signal voltage to said operating voltage setting circuit.

21. (Previously Presented) A semiconductor device according to claim 20,

wherein said functional circuit block comprises a register for temporarily storing said instruction or data and a functional block for computation, and

wherein said switch control circuit controls said register in accordance with said instruction or data inputted to said functional circuit block and said number of clock pulses counted.

22. (Previously Presented) A semiconductor device according to claim 15,

wherein said power status control circuit comprises an operating frequency setting circuit outputting clock pulses to said functional circuit block, said operating frequency setting circuit having a frequency divider, said frequency divider being able to vary a frequency dividing ratio,

wherein said prediction circuit comprises an input detection/clock counting circuit receiving said instruction or data and detecting the instruction or data which is inputted to said functional circuit block, counting a number of clock pulses inputted to said input detection/clock counting circuit, and controlling said frequency divider, and a setting register for storing a number of said clock pulses,

wherein, when said instruction or data is inputted to said functional circuit block, said input detection/clock counting circuit controls said operating frequency setting circuit to output clock pulses of a first frequency, and

wherein, when said input detection/clock counting circuit counts the number n of clock pulses that is stored in said setting register after said instruction or data is not inputted to said functional circuit block, said input detection/clock counting circuit

controls said operating frequency setting circuit to output clock pulses of a second frequency by increasing the frequency dividing ratio of said frequency divider.

23. (Previously Presented) A semiconductor device according to claim 22,

wherein said functional circuit block comprises a register for storing the input and a functional block for computation, and

wherein said input detection/clock counting circuit controls said register in accordance with said instruction or data and the number of clock pulses.

24. (Previously Presented) A semiconductor device according to claim 17, further comprising a circuit for updating said number n of clock pulses which the power status control circuit counts in accordance with a history.

25. (Previously Presented) A semiconductor device according to claim 24, further comprising a rewritable nonvolatile semiconductor memory for storing an update result.

26. (Previously Presented) A semiconductor device according to claim 15, further comprising a central processing unit comprising a power control table,

wherein said central processing unit outputs a control signal to said power status control circuit for controlling said power status control circuit by referring to said power control table, and outputs said instruction or data which is inputted to said functional circuit block.

27. (Previously Presented) A semiconductor device according to claim 26,

wherein said central processing unit further comprises a decoder for decoding a second instruction or data which is externally inputted to said central processing unit, said central processing unit outputting said control signal based on said second instruction or second data.

28. (Previously Presented) A semiconductor device according to claim 27, further comprising a plurality of said functional circuit block, and

wherein said power status of each of said plurality of functional circuit block is controlled by said control signal outputted by the central processing unit, which control signal is obtained by the decoding of said second instruction or data power controlling information by using said decoder.

29. (New) A semiconductor device comprising:

a functional circuit block for performing a processing when an instruction or data is inputted,

a power status control circuit for controlling a power status of said functional circuit block, and

a prediction circuit coupled to receive the instruction or data for controlling said power status control circuit, independently of other computation devices, based on said instruction or data which is inputted to both the functional circuit block and the prediction circuit,

wherein said power status control circuit comprises a power shutdown circuit for shutting down power which is supplied to said functional circuit block, said power shutdown circuit being coupled to said functional circuit block and a power supply,

wherein clock pulses are inputted into said functional circuit block and said power status control circuit,

wherein said prediction circuit comprises a counter for counting the number of clock pulses inputted to said functional circuit block and to said counter, a control circuit for controlling said power shutdown circuit, and an input detection circuit receiving the instruction or data inputted to said functional circuit block for detecting said instruction or data inputted to said functional circuit block,

wherein said counter outputs a first signal to said control circuit when a number of said clock pulses counted is n,

wherein, when there is no instruction or data inputted to said functional circuit block, said input detection circuit outputs a reset signal to said counter to reset a counting of said clock pulses and outputs a second signal to said control circuit, and said control circuit outputs an output signal of a first state to shut down said power supplied to said functional circuit block when both said first and second signals are inputted to said control circuit,

wherein said functional circuit block comprises a register for temporarily storing said instruction or data and a functional block for computation, and

wherein said prediction circuit further comprises a comparator for controlling said register by comparing the output of said control circuit with the number of clock pulses inputted to said comparator and a predetermined number, said comparator

starting a counting of said clock pulses when said control circuit outputs said output signal of a second state.